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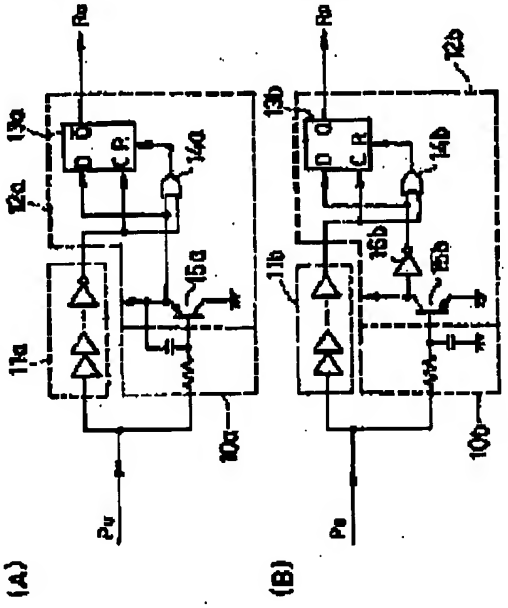
(54)【発明の名称】　PLL回路

(57)【要約】
【目的】　受信システムの周波数シンセサイザにおけるPLL回路のS／N改善のために位相比較にデッドゾーンを設けつつ安定な同期収束を可能とする。
【構成】　位相進みPDパルスを遅延器11bで遅延してD－FF13bのクロック入力とする。また、PDパルスを時定数回路10bで積分し、この積分波形をトランジスタ15bの閾値と比較してこの閾値以上のときにパルスを生成する。このパルスをD－FF13bのデータ入力としてPDパルスをラッチし、オアゲート14bでPDパルス消滅時にD－FF13bをリセットする。このQ出力RDをチャージポンプ、ループフィルタへ供給してVCOの制御電圧を得る。
【効果】　デッドゾーンは時定数回路のCRとトランジスタの閾値で定まり、デッドゾーンより大なるPDパルスはそのまま出力されるので、同期収束が安定となる。



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【特許請求の範囲】

【請求項１】　電圧制御発振手段と、この発振出力周波数信号と外部より入力される基準周波数信号との位相比較をなす位相比較手段と、この位相比較出力に応じて前記電圧制御発振手段の制御電圧を生成する制御電圧生成手段とを含むＰＬＬ回路であって、前記制御電圧生成手段は、前記位相比較出力を遅延する遅延手段と、前記位相比較出力を入力とする時定数回路と、前記遅延手段の出力によって前記時定数回路の出力状態をラッチし前記遅延手段の出力が消失したときにこのラッチ状態を解除するラッチ手段とを含み、このラッチ出力を用いて前記制御電圧を生成するよう構成されていることを特徴とするＰＬＬ回路。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はＰＬＬ（フェイズロックドループ）回路に関し、特に変復調技術における安定な同期信号を得るために用いられるＰＬＬ回路に関する。

【０００２】

【従来の技術】ＰＬＬ回路は、外部から与えられる基準周波数信号と、ＶＣＯ（電圧制御発振器）の発振出力を分周した分周出力との位相差を検出し、その位相差に応じた直流電圧によりＶＣＯを制御して安定な発振出力を得るものである。

【０００３】受信システムにおいて、この発振出力をローカル発振信号として受信ＲＦ信号と混合し、ＩＦ信号を作成するようになっており、チャンネル切換え時の周波数切換えには、分周器（プログラムデバイダ）の分周比を変更するか、あるいは基準周波数信号自体を信号源にダイレクトディジタルシンセサイザ等を用いて変化させることにより同調を得ている。

【０００４】局発発振周波数シンセサンザにおいては、高速の周波数切換えのためには、系の高利得設計が行われるが、その反面帰還帯域幅が大きくなり、系内に雑音を取り込み易く、発振出力のＣ／Ｎ値が問題となる。こうした場合にネガティブな措置として、位相比較における不感帯（デッドゾーン）を拡げる方法がとられる。

【０００５】図５は特開昭６３－２６０３１７号公報に示された従来のＰＬＬ回路の位相比較器の部分を示す回路図であり、２１はチャージポンプ、２２は第１のＤ－ＦＦ、２３は第２のＤ－ＦＦ、２４は第１のＤ－ＦＦ２２のクロック入力端子に印加された基準周波数信号ｆＲを遅延する第１の遅延回路、２５は第２のＤ－ＦＦ２３のクロック入力端子に印加された分周信号ｆＰを遅延する第２の遅延回路である。２５，２４は遅延回路であり、２８，２９はデッドゾーン拡大信号Ｄｚに応じて遅延量を選択する回路である。

【０００６】次に動作について説明する。Ｄ－ＦＦ２２の入力端子Ｄ１には、Ｄ－ＦＦの反転出力Ｑ２が印加され、Ｄ－ＦＦ２３の入力端子Ｄ２にはＤ－ＦＦ２２の反転出力Ｑ１が印加され、出力Ｑ１はチャージポンプ回路

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２１のＮＭＯＳ２６のゲートに印加され、出力Ｑ２はＮＭＯＳ２７のゲートに印加される。

【０００７】デッドゾーン拡大信号Ｄｚをオフ（"０"）にすると、遅延回路の最終段の遅延信号が選択回路２８，２９より選択される。

【０００８】まず、分周信号ｆＰに対して基準周波数信号ｆＲの位相が一致しているとき、図６（Ａ）に示す様にｆＰとｆＲの立上りにより、Ｄ－ＦＦ２２，２３は共に互いの反転出力"１"を取込んで各々出力Ｑ１及びＱ２に出力する。この出力Ｑ１及びＱ２は、図６（Ｃ）の様に実線で示される傾斜で上昇し、スレッショルド電圧Ｖｔに達する時点ＴＤで選択回路２８，２９の出力Ｒ１とＲ２が立上る。

【０００９】すなわち、遅延回路２４，２５の最大遅延量はＴＤと等しくなる様に設計してあり、出力Ｒ１，Ｒ２によりＤ－ＦＦ２２，２３は共にリセットされ、出力Ｑ１及びＱ２は低下し、従ってこの場合、ＮＭＯＳ２６，２７は共にオンせず、位相差に応じた出力ＰＤは出力されない。

【００１０】図６（Ｂ）で示される如く、ｆＲ´がｌｏｎｓｅｃ早くなった状態では、Ｄ－ＦＦ２２は"１"を取込み、出力Ｑ１は（Ｃ）の点線㋑の様に立上る。Ｄ－ＦＦ２３はｌｏｎｓｅｃ遅れてｆＰの立上りで"１"を取込み、その出力Ｑ２が上昇する。次に選択回路２８からＲ１´が出力されると、Ｄ－ＦＦ２３はリセットされ、出力Ｑ２はＶｔに達する前に、（Ｃ）の破線㋺の様に立下がる。

【００１１】一方、Ｄ－ＦＦ２２の出力Ｑ１はＶｔに達し、選択回路２９の出力Ｒ２によりＤ－ＦＦ２２がリセットされることになる。従って、出力Ｑ１がＶｔ以上になった期間、ＮＭＯＳ２８がオンとなって、位相差に応じた出力ＰＤ"０"が出力される。すなわち、図６（Ｃ）の場合には、ｆＲが早くなると、出力Ｒ２が出力される前に必ずＶｔに達することになり、デッドゾーンは零となるのである。

【００１２】次に図６（Ｄ）はＤｚ＝"１"の場合であり、Ｄｚ＝"０"の時より、遅延量の少い遅延信号が選択される。故ずｆＲとｆＰの位相が一致している時には、遅延回路の出力Ｒ１とＲ２が発生するのがＴＤより早くなるので、Ｑ１とＱ２はＶｔに達せずにＤ－ＦＦ２２，２３がリセットされる。

【００１３】いま、出力Ｒ１とＲ２がＴＤよりｌｏｎｓｅｃ早い遅延信号であるとした時、ｆＲが図６（Ｄ）の如く、ｌｏｎｓｅｃ早くなった場合、Ｄ－ＦＦ２２の出力Ｑ１は（Ｄ）の実線で示される如く上昇し、Ｖｔに達する直前において、出力Ｒ２が発生するためにＤ－ＦＦ２２がリセットされ、Ｑ１は低下する。

【００１４】したがって、図６（Ｅ）の場合には、ｆＲとｆＰの位相差がｌｏｎｓｅｃ以内では、出力Ｑ１がＶｔに達する前に必ずＤ－ＦＦ２２がリセットされること

になり、NMOS26がオンとなって位相差に対応する出力Pdが発生されることはない。すなわち、10nsecのデッドゾーンが設けられる。同様にfPがfRより早くなった場合は、10nsec以下であれば、D－FF23の出力Q2がVtに達する前にD－FF23がリセットされるので、10nsecのデッドゾーンが発生する。

【0015】デッドゾーンを設けることにより、PLL回路がロックしている状態でVCOの外乱となるような制御パルスの頻繁な発生が防止され、またジッタノズル等の雑音信号もカットされ、S／Nを大幅に改善している。

【0016】

【発明が解決しようとする課題】上述した従来の位相比較回路で構成したPLL回路においては、デッドゾーン近傍での位相差に対して、系の反応が鈍化する問題がある。

【0017】例えば、fRがfPに対して12nsec早くなった場合を想定すると、図7に示す様になる。Dz＝"0"のデッドゾーン0の状態では、出力Q1がVtを越えている時間は約12nsecとみることができ、Pd信号として"1"が12nsec出力されるが、Dz＝"1"のデッドゾーン10nsecの状態では、出力Q1がVtを越える時間約2nsecとなり、Pd信号として「1」は2nsec間しか現れず、ループフィルタを通してのVCOの制御を行う積分電圧値の変化の割合が鈍くなる。

【0018】この位相比較の特性を図に示すと図8のようになる。fRとfPの位相差が大きい時には、相対的にみてそのデッドゾーン設定分の10nsecで削られる時間が小さくなるため、影響は少くなるが、デッドゾーン近傍でかなり系としての感度は劣化する。

【0019】具体的には、PLL回路の発振周波数の切換時、シフト周波数付近への変化に支障はないが、収束値付近での回路に影響が出て、収束値に対して振動が尾を引く現象が生じ易い問題点がある。

【0020】本発明の目的は、位相比較時にデッドゾーンを設けつつ安定な同期収束を可能としたPLL回路を提供することである。

【0021】

【課題を解決しようとする手段】本発明によれば、電圧制御発振手段と、この発振出力周波数信号と外部発振周波数信号との位相比較をなす位相比較手段と、この位相比較出力に応じて前記電圧制御発振手段の制御電圧を生成する制御電圧生成手段とを含むPLL回路であって、前記制御電圧生成手段は、前記位相比較出力を遅延する遅延手段と、前記位相比較出力を入力とする時定数回路と、前記遅延手段の出力によって前記時定数回路の出力状態をラッチし前記遅延手段の出力が消失したときにこのラッチ状態を解除するラッチ手段とを含み、このラッチ出力を用いて前記制御電圧を生成するよう成されていることを特徴とするPLL回路が得られる。

【0022】

【実施例】以下に本発明の実施例について図面を参照しつつ詳細に説明する。

【0023】図1は本発明の実施例のブロック図であり、基準周波数fRを発生する発振器1の出力は位相比較器3の一入力となる。この位相比較器3の他入力には、VCO7の発振周波数を分周器2にて分周した周波数fPの信号が印加されている。

【0024】位相比較器3からは、位相差に応じたパルス幅の進み信号Pdと遅れ信号Puとが出力され、フィルタ回路4a，4bへ夫々入力される。このフィルタ回路4a，4bが本発明の特徴部分の回路であって図2にその一具体例が示されている。このフィルタ回路4a，4bにおいて、デッドゾーンが設定されつつPd，Puのパルス幅（位相差情報を含んでいる）が変化することのない、位相差信号RU，RDが生成される。

【0025】この位相差信号RU，RDはチャージポンプ5を介してループフィルタ6へ入力され積分されることによりVCO7の制御電圧となる。

【0026】このVCO7の出力が受信システムにおけるローカル発振周波数となっており、受信チャンネルの切換え指令に応答して基準周波数発振器1の発振周波数fR及びプログラムデバイダ2の分周比がコントロールされ、PLL周波数シンセサイザを構成している。

【0027】図2（A），（B）は図1のフィルタ回路4a，4bの各具体例回路図である。まず、図2（A）を参照すると、進み信号Puは遅延回路11a及び時定数回路10aへ夫々入力される。遅延回路11aの遅延出力は、ラッチ回路12aを構成するD－FF12aのクロック入力となる。

【0028】時定数回路10aの出力は、ラッチ回路12aを構成するPNPトランジスタ15aのベース入力となり、このトランジスタ15aのエミッタ出力はD－FF13aのデータ入力となると共に、オアゲート14aの一入力となる。このオアゲート14aの他入力には遅延回路11aの遅延出力が印加され、オア出力はD－FF13aのリセット入力となっている。そして、D－FF13aの反転Q出力がRUとなる。

【0029】図2（B）は遅れ信号Pd側についても、具体的に遅延回路11b，時定数回路10b及びラッチ回路12bからなっているが、時定数回路10bの電源ラインの極性，ラッチ回路内のトランジスタ15bの極性が進み信号Pu側とは逆となっており、また、トランジスタ15bのコレクタ出力はインバータ16bにて極性反転されてD－FF13bのデータ入力及びオアゲート14bの一入力となっている。

【0030】図3は図2（B）の回路の動作を示す各信号波形図であり、fRがfPに対して位相が遅れたと

合、遅れ信号Pdが出力された場合のものであって、本例では遅れ度合が異なる2つのPdパルスを示している。

【0031】（C）に示すPdパルスは時定数回路10bの時定数によって（d）に示す立上りの緩やかな波形（積分波形）に変換される。この波形がトランジスタ15bの閾値Vtに達しないPdパルスでは、トランジスタ15bはオンせず、よってインバータ16bからD－FF13bへのデータ入力信号（D入力信号）は生成されない。一方、積分波形が閾値Vtに達するPdパルスでは、トランジスタ15bはオンしてインバータ16bからデータ入力信号が（e）に示す如く生成され、このデータ入力信号は積分波形が閾値Vtより小となるまで生成される。

【0032】D－FF13bのクロック入力にはPdパルスが時間tDだけ遅延された（f）に示す如き遅延Pdパルスが供給されている。ここで、遅延時間tDと時定数回路10bの時定数により定まる時間tM（図（e）参照）とを略々同一か若しくはtMをtDより若干小に設定しておけば、クロック信号（遅延パルスPd）の立上りタイミングに同期しD－FF13bにはデータ入力信号が取込まれてラッチされる。

【0033】遅延Pdパルスが立下がると、オアゲート14bの出力によりD－FF13bはリセットされるので、ラッチ状態がリセットされ、結果として（g）に示すフィルタ回路出力RDが得られることになる。

【0034】従って、位相差に応じた進み信号Pdは、その位相差の度合によってはフィルタ回路4b（図1）を通すことにより後段のチャージポンプ5へ入力されることなく、よってフィルタ回路12bの閾値Vtにより定まる時間tMがデッドゾーンとなるのである。

【0035】デッドゾーンを越える位相進み信号Pdについては、そのパルスの波形が変化することなくチャージポンプ5へ出力されるで、デッドゾーン近傍において、VCO7の制御を行う積分電圧値の変化の割合が、従来の如く鈍くなることがないので、位相比較特性としては図4に示すものが得られる。

【0036】尚、フィルタ回路4a、4bの出力RU，RDのPU，Pdに対する遅延時間TDについては、デッドゾーンtMを100ns（10MHz）またはそれ以上としても、ローカル発振周波数のチャンネル切換え

時に要求される収束時間（1ms以下のオーダ）に比し無視できる。

【0037】図2の回路は一例に示すに止まるもので、種々の回路変形が可能であることは明らかである。

【0038】

【発明の効果】以上のべた様に、本発明によれば、PLL受信システムにおいて要求される高速チャンネル切換えのために高利得でPLLを設計した場合にも、位相比較におけるデッドゾーンを設定しつつチャンネル切換え時に収束値近傍での振動や引き込み現象を伴うことのない高性能PLL回路が実現できるという効果がある。

【0039】定量的に述べると、S／N値で10dB以上の改善があり、チャンネル切換え収束時間で2ms以上の短縮が図れるものである。

【図面の簡単な説明】

【図1】本発明によるPLL回路のブロック図である。

【図2】図1のフィルタ回路4a，4bの一例を示す回路図である。

【図3】図2の回路の各部動作波形図である。

【図4】本発明によるPLL回路の位相比較特性図である。

【図5】従来のPLL回路の位相比較器の回路図である。

【図6】図5の回路の各部作波形図である。

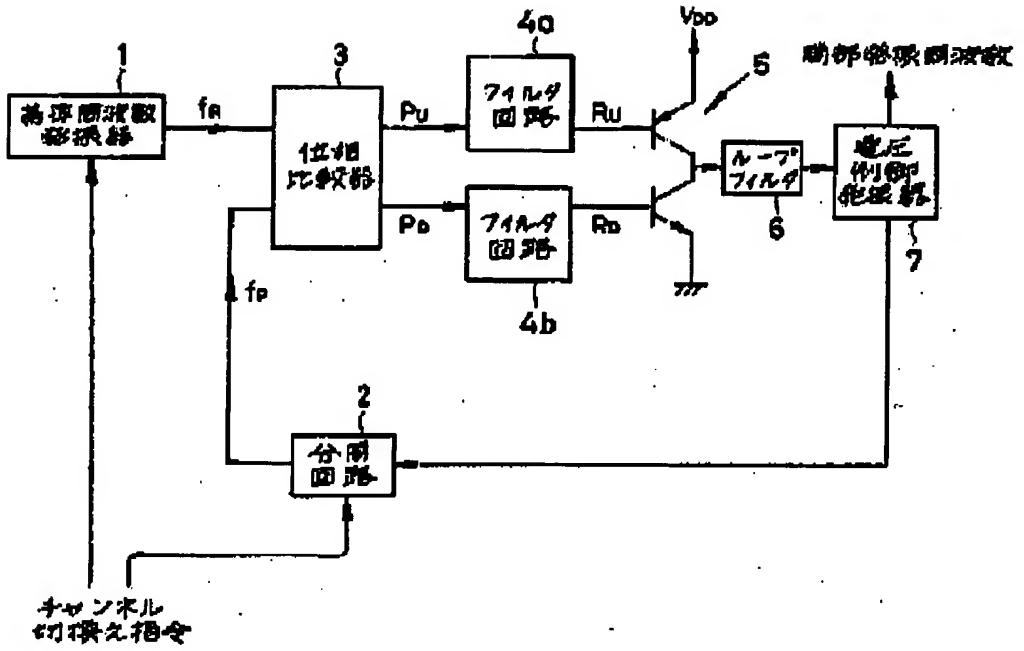
【図7】図5の回路の各部作波形図である。

【図8】図5の回路の位相比較特性図である。

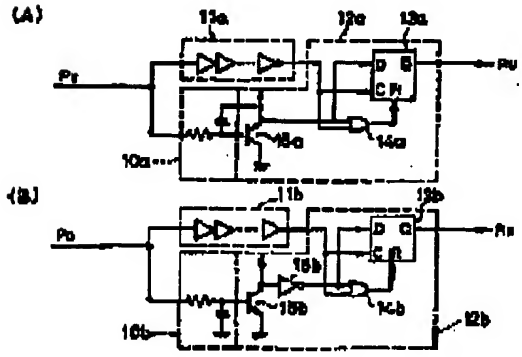
【符号の説明】

1　基準周波数発振器
2　分周器
3　位相比較器
4a，4b　フィルタ回路
5　チャージポンプ
6　ループフィルタ
7　VCO
10a，10b　時定数回路
11a，11b　遅延回路
12a，12b　ラッチ回路
13a，13b　D－FF
14a，14b　オアゲート
15a，15b　トランジスタ
16b　インバータ

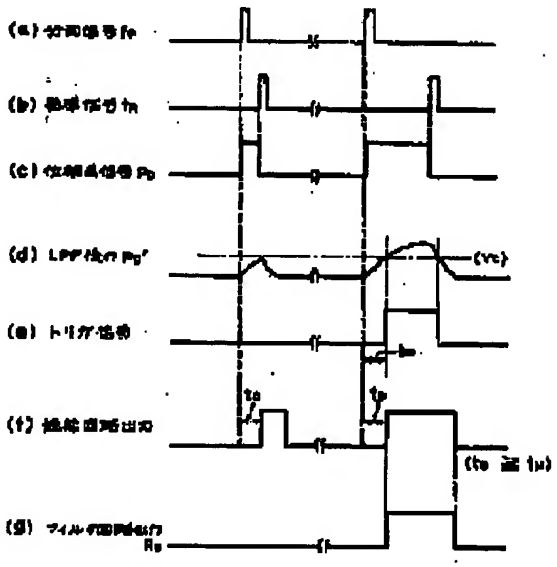
【図1】



【図2】



【図3】



【図4】

【図5】

【図6】

【図7】

【図8】

【手続補正 】
【提出日】平成6年1月10日
【手続補正1】
【補正対象書類名】明細書
【補正対象項目名】発明の名称
【補正方法】変更
【補正内容】
【発明の名称】 ＰＬＬ回路
【手続補正2】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】追加
【補正内容】
【特許請求の範囲】
【請求項１】 電圧制御発振手段と，この発振出力周波数信号と外部発振周波数信号との位相比較をなす位相比較手段と，この位相比較出力に応じて前記電圧制御発振手段の制御電圧を生成する制御電圧生成手段とを含むＰＬＬ回路であって，前記制御電圧生成手段は，前記位相比較出力を遅延する遅延手段と，前記位相比較出力を入力とする時定数回路と，前記遅延手段の出力によって前記時定数回路の出力状態をラッチし前記遅延手段の出力が消失したときにこのラッチ状態を解除するラッチ手段とを含み，このラッチ出力を用いて前記制御電圧を生成するよう構成されていることを特徴とするＰＬＬ回路。
【請求項２】 前記位相比較手段は，前記発振出力周波数信号と外部発振周波数信号との一方に対する他方の位相ずれを検出して位相進み及び位相遅れに夫々対応した位相比較出力を生成するよう構成されており，前記遅延手段，前記時定数回路及びラッチ手段の各々は前記位相進み及び位相遅れに対応した位相比較出力に夫々対応して設けられていることを特徴とする請求項１記載のＰＬＬ回路。
【請求項３】 前記遅延手段の遅延時間は，前記位相比較における不感帯（デッドゾーン）に相当する時間に設定されていることを特徴とする請求項１または２記載のＰＬＬ回路。

【手続補正３】
【補正対象 類名】明細書
【補正対象項目名】０００６
【補正方法】変更
【補正内容】
【０００６】次に動作について説明する。Ｄ－ＦＦ２２の入力端子Ｄ1には，Ｄ－ＦＦ２３反転出力Ｑ2が印加され，Ｄ－ＦＦ２３の入力端子Ｄ2にはＤ－ＦＦ２２の反転出力Ｑ1が印加され，出力Ｑ1はチャージポンプ回路２１のＮＭＯＳ２６のゲートに印加され，出力Ｑ2はＮＭＯＳ２７のゲートに印加される。
【手続補正４】
【補正対象書類名】明細書
【補正対象項目名】００１５
【補正方法】変更
【補正内容】
【００１５】デッドゾーンを設けることにより，ＰＬＬ回路がロックしている状態でＶＣＯの外乱となるような制御パルスの頻繁な発生が防止され，またジッタノイズ等の雑音信号もカットされ，Ｓ／Ｎを大幅に改善している。
【手続補正５】
【補正対象書類名】明細書
【補正対象項目名】００１７
【補正方法】変更
【補正内容】
【００１７】例えば，ｆＲがｆＰに対して１２ｎｓｅｃ早くなった場合を想定すると，図７に示す様になる。Ｄｚ＝"０"のデッドゾーン０の状態では，出力Ｑ1がＶｔを越えている時間は約１２ｎｓｅｃとみることができ，ＰＤ信号として"１"が１２ｎｓｅｃ出力されるが，Ｄｚ＝"１"のデッドゾーン１０ｎｓｅｃの状態では，出力Ｑ1がＶｔを越える時間は約２ｎｓｅｃとなり，ＰＤ信号として「１」は２ｎｓｅｃ間しか現れず，ループフィルタを通してのＶＣＯの制御を行う積分電圧値の変化の割合が緩くなる。

PATENT ABSTRACTS OF JAPAN

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TOTTORI SANYO ELECTRIC CO LTD
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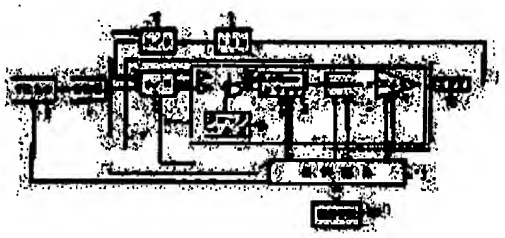
(54) PLL SYNTHESIZER

(57)Abstract:
PURPOSE: To provide the PLL synthesizer consisting of parts where charge pump control and storage are easy.
CONSTITUTION: A charge pump 6 consists of an up/down counter 9 which counts the phase difference between an up signal Pu and a down signal Pd of a phase comparator 5, a latch 10 where the output value of the up/down counter 9 is held, and a digital-analog converter 11 which converts the output of the latch 10 into an analog signal. Thus, power saving and temperature correction are facilitated, and the strength against noise is improved. For the purpose of shortening the lock-up time, it is unnecessary to prepare ana switch two charge pumps or to propare and switch two resistances.



LEGAL STATUS

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[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

* NOTICES *

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CLAIMS

[Claim(s)]

[Claim 1] A voltage controlled oscillator and the programmable divider which carries out dividing of the output of this voltage controlled oscillator in adjustable, The phase comparator which outputs the rise signal Pu which detects the phase contrast of the output from reference frequency VCO and this frequency VCO, and the output of a programmable divider, and shows this phase contrast by pulse width, and the down signal Pd, In the PLL synthesizer which consisted of low-pass filters which change into the control voltage to a voltage controlled oscillator the voltage of the charge pump which changes the rise signal Pu from this phase comparator, and the down signal Pd into voltage, and this charge pump The counter the aforementioned charge pump counts [counter] the phase contrast of the aforementioned rise signal Pu and the down signal Pd, The PLL synthesizer characterized by consisting of a latch holding the output value of this counter, and a digital analog converter which changes the output of this latch into an analog signal.

[Claim 2] The PLL synthesizer indicated to the claim 1 characterized by having the control circuit which controls change of the aforementioned control voltage based on a storage means to memorize the data concerning the output of the aforementioned counter, and this storage means.

[Claim 3] The PLL synthesizer indicated to the claim 1 characterized by having the control circuit which has by the output value of the aforementioned counter corresponding to the division ratio changed based on the aforementioned storage means, and controls the aforementioned latch when there are a storage means to memorize the correlation of the output value of the aforementioned counter and the division ratio of a programmable divider, and change of a division ratio.

[Claim 4] It is the PLL synthesizer indicated to the claim 1 characterized by having a control circuit and a storage means, outputting the output of the latch which the aforementioned control circuit made the aforementioned storage means memorize the output of a latch, and was memorized by the aforementioned storage means to a digital analog converter, and intercepting at least one between a voltage controlled oscillator and a digital analog converter.

[Claim 5] It is the PLL synthesizer indicate holding the output-control voltage of the aforementioned low-pass filter in front of power-saving operation to the claim 1 carry out as the feature by making the aforementioned programmable divider into non-actuation by having the control circuit to which power-saving operation is made to perform, and a storage means, and the aforementioned control circuit's making the aforementioned storage means memorize the output of the aforementioned counter in front of power-saving operation, and controlling the aforementioned latch based on the aforementioned storage means at the time of power-saving operation.

[Claim 6] The PLL synthesizer indicated to the claim 1 characterized by having the control circuit which has by the output value of the aforementioned counter in a predetermined division ratio based on a storage means to memorize the correlation of the temperature of the reference frequency VCO in which temperature compensation is possible, and the output value of the aforementioned counter in a predetermined division ratio and reference frequency VCO, and the aforementioned storage means, and carries out temperature compensation of the reference frequency VCO.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the PLL synthesizer which has a charge pump.
[0002]
[Description of the Prior Art] Many PLL synthesizers to radio, portable telephone, etc. are used. There is a charge pump which changes the phase contrast signal from a phase comparator into the voltage to a low-pass filter in this PLL synthesizer. This charge pump consists of two FET (Field Effect Transisitor) so that it may be indicated by JP,58-22343,Y. Operation of a charge pump is explained. Drawing 5 is a block diagram of a PLL synthesizer which has a charge pump (15) as shown in drawing 6 , and drawing 7 is a timing chart which shows operation of a phase comparator (phi/D) (5) and a charge pump (15). fp of these drawings is the output from a voltage controlled oscillator by which dividing was carried out by the programmable divider, and fr is the output from reference frequency VCO by which dividing was carried out with the counting-down circuit. If fp and fr are inputted into a phase comparator, only while the phase of fp is progressing rather than fr, the rise signal Pu of a phase comparator serves as Low, and while the phase of fp is behind fr, the down signal Pd of a phase comparator serves as Low. If each of fp(s) and fr(s) is High(s), each FET of both of a charge pump is in an OFF state, and the capacitor of a low-pass filter (12) holds fixed potential, and holds a lock. However, when Pu is set to Low, the capacitor of a low-pass filter (12) is made to charge, and when Pd is set to Low, the capacitor of a low-pass filter is made to discharge. In this way, the always stabilized oscillation frequency can be obtained from a voltage controlled oscillator.
[0003]
[Problem(s) to be Solved by the Invention] Since the conventional charge pump consisted of FET of the above analogs, it was not easy to control by the control circuit or to memorize the value of a charge pump. For this reason, based on the value of a charge pump, control of PLL operation, such as power saving and temperature compensation, was difficult. Moreover, since control of a charge pump was difficult, the conventional PLL control had the problem of taking lock-up time for a long time, when a change of a division ratio was made greatly, in order to start feedback control from the state at that time, when a change of a division ratio is made.
[0004] Furthermore, since the charge pump of the conventional example had amended the control voltage of a low-pass filter by charge and electric discharge like ****, the time constant of a low-pass filter (12) needed to be changed to shortening lock-up time. For this reason, as shown in drawing 8 , a charge pump (15) and two (16) were prepared, this needed to be changed by the CONT signal, and two resistance needed to be prepared and this needed to be changed with a switch (17).
[0005]
[Means for Solving the Problem] this invention was made in view of this point, and the 1st feature is that a charge pump consists of a counter which counts the phase contrast of the aforementioned rise signal Pu and the down signal Pd, a latch holding the output value of this counter, and a digital analog converter which changes the output of this latch into an analog signal.
[0006] The 2nd feature is having had the control circuit which controls change of the aforementioned control voltage based on a storage means memorizing the data concerning the output of the aforementioned counter, and this storage means.
[0007] The 3rd feature is having the control circuit which has by the output value of the aforementioned counter corresponding to the division ratio changed based on the aforementioned storage means, and controls the aforementioned latch, when a storage means to memorize the correlation of the output value of the aforementioned counter and the division ratio of a programmable divider, and change of a division ratio are.
[0008] It is the 4th feature's being equipped with a storage means, outputting the output of the latch which the aforementioned control circuit's made the aforementioned storage means memorize the output of a latch, and was memorized by the aforementioned storage means to a digital analog converter, and intercepting at least one between a voltage controlled oscillator and a digital analog converter.

[0009] It is holding the output-control voltage of the aforementioned [illegible] equipping the 5th feature with the control circuit to which power-saving operation is made to perform by making a programmable divider into non-actuation, and a storage means, and the aforementioned control circuit's making the aforementioned storage means memorize the output of the aforementioned counter in front of power-saving operation, and controlling the aforementioned latch based on the aforementioned storage means at the time of power-saving operation.
[0010] The 6th feature is having the control circuit which has by the output value of the aforementioned counter in a predetermined division ratio based on a storage means memorizing the correlation of the temperature of the reference frequency VCO in which temperature compensation's is possible, and the output value of the aforementioned counter in a predetermined division ratio and reference frequency VCO, and the aforementioned storage means, and carries out temperature compensation of the reference frequency VCO.
[0011]
[Function] Storage of control or an output is easy and can constitute a charge pump. Thereby, temperature compensation of power saving which makes a programmable divider non-actuation, shortening of lock-up time, and the reference frequency VCO is carried out.
[0012]
[Example] The example of this invention is explained based on drawing. Drawing 1 is the block diagram of a PLL synthesizer. (1) is a voltage controlled oscillator (VCO) and it outputs desired frequency outside. (2) is a programmable divider (P/D) and it carries out dividing of the output of a voltage controlled oscillator (1) in adjustable. (3) is a temperature compensated crystal oscillator (TCXO), and it can tune oscillation frequency finely. (4) is a counting-down circuit and it carries out dividing of the output of a temperature compensated crystal oscillator (3). (5) is a phase comparator (phi/D) and it outputs the phase contrast of the output fr of a temperature compensated crystal oscillator (3) by which dividing was carried out to the output fp of a voltage controlled oscillator (1) by which dividing was carried out, and detection of a lock. Phase contrast is outputted by the rise signal Pu and the down signal Pd. (6) is a charge pump and it changes the rise signal Pu from a phase comparator (5), and the down signal Pd into voltage. A charge pump (6) is aligned with a phase comparator (5), and it is called the phase comparator (7) of a wide sense. On the other hand, (5) which does not contain a charge pump (6) is a phase comparator in a narrow sense. Here, a phase comparator in a narrow sense is only called phase comparator.
[0013] A charge pump (6) consists of a clock pulse (8), an updown counter (Up/Down counter) (9), and a latch (Latch) (10) and a digital analog converter (11) (DAC). An updown counter (9) counts each phase contrast from the rise signal Pu from a phase comparator (5), and the down signal Pd. A clock pulse (8) sends out the reference pulse signal for the count of an updown counter (9). A latch (10) holds the output of an updown counter (9). That is, the output of an updown counter (9) is temporarily memorizable. A digital analog converter (11) changes into the voltage according to counted value the output of the latch (10) which is a digital signal. (12) is a low-pass filter (LPF) and amends the control voltage to a voltage controlled oscillator (1) based on the output voltage of a digital analog converter (11).
[0014] (13) is a control circuit and controls each part. (14) is storage meanses, such as RAM and ROM, and memorizes data required for operation of a control circuit (13). For example, the correlation of the division ratio to the output of an updown counter (9) or temperature is memorized.
[0015] 12 is a timing chart which shows operation of a phase comparator (5) and an updown counter (9). If the output fp of a programmable divider (2) and the output fr of a counting-down circuit (4) are inputted into a phase comparator (5), only while the phase of fp is progressing rather than fr, the rise signal Pu of a phase comparator (5) serves as Low, and while the phase of fp is behind fr, the down signal Pd of a phase comparator (5) serves as Low. The pulse width of Low of Pu and Pd shows the phase contrast of fp and fr. This pulse width is changed into the signal (Pu' and Pd') expressed with the pulse width of High by the clock pulse (8) and the logical element (an inverter and AND gate). An updown counter (9) counts the pulse number of this Pu' and Pd', and outputs the value as a DESHITARU signal. The digital-output signal of an updown counter (9) is held by latch (10), and is changed into the voltage (analog) according to counted value (phase contrast) by the digital analog converter (11). The control voltage of a low-pass filter (12) is amended on this voltage.
[0016] Thus, if the phase of fp is progressing rather than fr, while the control voltage of a low-pass filter (12) was raised and the phase of fp is behind fr, the control voltage of a low-pass filter (12) is dropped. In this way, the always stabilized oscillation frequency can be obtained from a voltage controlled oscillator.
[0017] The above is the basic composition and basic operation of this invention, and has the following features.
[0018] ** Since the charge pump of the conventional example had amended the control voltage of a low-pass filter (12) by charge and electric discharge, it needed to change the time constant of a low-pass filter (12) to shortening lock-up time. For this reason, as shown in drawing 8 , two charge pumps were formed, this needed to be changed, and two resistance needed to be prepared and this needed to be changed. However, since the charge pump of this invention generates direct voltage, and in order for the speedup / speed down of applied voltage to a voltage controlled oscillator (1) to be dependent on the speed of a clock pulse (8), it is not necessary to take into consideration the time constant of a low-pass filter (12), and it has

neither a charge pump nor resistance doubly like before, or operation

[0019] * Since the processing inside a charge pump (6) is a digital signal, the digital control which used a microcomputer, RAM, the logical element, etc. is easy.

[0020] ** When a change of a division ratio is made, in order to start feedback control from the state at that time, the conventional PLL control takes lock-up time for a long time, when a change of a division ratio is made greatly. The control circuit (13) of this invention reads the correlation of a division ratio and the output value of an updown counter (9) from a storage means (14), when a setting change of a division ratio is made in a key stroke etc. (Y of S1), as shown in drawing 3 (S2). The tabular format of the updown counter (9) output value corresponding to the division ratio of it that is sufficient as a correlation, and the function by statistics, such as the least square method, is sufficient as it. By this correlation, the change value of the updown counter (9) corresponding to the change value of a division ratio is calculated, and this value is outputted to an updown counter (9) (S3). Feedback operation of PLL is performed by making this value into initial value (S4).

[0021] Furthermore, it has with the lock-up signal from a phase comparator (5) by the output value of (Y of S5), and the updown counter at this time (9), and the data of the aforementioned correlation of a storage means (14) are updated (S6). (study)

[0022] Unless it carried out operation by the loop conventionally, the convergence value of attenuation was not found. However, since an updown counter (9) and a latch (10) are digital signals, this invention can output the voltage assumed easily from a charge pump (6). For this reason, lock-up time can be shortened and especially the effect when a change of a division ratio is made greatly is greatest.

[0023] ** Since an output is digital, a clock pulse (8) and a latch (10) are easy for a control circuit (13) to input into the next circuit the output value which made the storage means (14) memorize this output value, and made it memorize. And even if it intercepts between a voltage controlled oscillator (1) and a charge pump (6), the control voltage of a low-pass filter (12) can be held.

[0024] For example, as shown in drawing 4 , if the lock signal from a phase comparator (5) is received (S7), a control circuit (13) will make a storage means (14) memorize the output value of a latch (10) (S8), will read this output value from a storage means (14), and will output it to a digital analog converter (11) (S9). And between a latch (10) and digital analog converters (11) is intercepted (S10), and between a phase comparator (5) and charge pumps (6) is intercepted (S11). Next, supply (not shown) of the power supply to a programmable divider (2) is intercepted, and this is made into non-actuation (S12).

[0025] Thus, although a loop is intercepted and a programmable divider (2) serves as non-actuation, the control voltage of a low-pass filter (12) can be held by the output value of the latch (10) memorized. And by intercepting a loop, even if the noise by change of a phase comparator (5) is lost and a noise arises, a noise cannot carry out a loop and a PLL synthesizer strong against a noise can be supplied. Furthermore, power consumption can be lessened by making a programmable divider (2) into non-actuation.

[0026] an above-mentioned example -- especially -- power consumption -- although the large programmable divider (2) was made into non-actuation, even if it makes a counting-down circuit (4), a phase comparator (5), and an updown counter (9) into non-actuation, the output-control voltage of a low-pass filter can be held

[0027] Moreover, although DAC (11) was controlled by the above-mentioned example based on the output value of a latch (10), based on the output value of an updown counter (9), you may control a latch (10) (9).

[0028] ** Carry out small change of the frequency outputted from reference frequency VCO with temperature. For this reason, the control circuit (13) makes the storage means (14) memorize the correlation of the output value of an updown counter, and the temperature of reference frequency VCO in a predetermined division ratio beforehand. And temperature compensation of the reference frequency VCO is carried out to the division ratio set up from the output value of an updown counter using the correlation read from the storage means (14). Thereby, a temperature control with a high precision becomes possible.

[0029]

[Effect of the Invention] Since the processing inside a charge pump (6) is a digital signal, the digital control which used a microcomputer, RAM, the logical element, etc. is easy. This storage and control can perform power saving and temperature compensation. Moreover, a PLL synthesizer strong against a noise can be supplied.

[0030] Furthermore, in order to shorten lock-up time, two charge pumps are formed and the cure which changes this, or prepares two resistance and changes this is not needed.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] this invention relates to the PLL synthesizer which has a charge pump.

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PRIOR ART

[Description of the Prior Art] Many PLL synthesizers to radio, portable telephone, etc. are used. There is a charge pump which changes the phase contrast signal from a phase comparator into the voltage to a low-pass filter in this PLL synthesizer. This charge pump consists of two FET (Field Effect Transisitor) so that it may be indicated by JP,58-22343,Y. Operation of a charge pump is explained. Drawing 5 is a block diagram of a PLL synthesizer which has a charge pump (15) as shown in drawing 6 , and drawing 7 is a timing chart which shows operation of a phase comparator (phi/D) (5) and a charge pump (15). fp of these drawings is the output from a voltage controlled oscillator by which dividing was carried out by the programmable divider, and fr is the output from reference frequency VCO by which dividing was carried out with the counting-down circuit. If fp and fr are inputted into a phase comparator, only while the phase of fp is progressing rather than fr, the rise signal Pu of a phase comparator serves as Low, and while the phase of fp is behind fr, the down signal Pd of a phase comparator serves as Low. If each of fp(s) and fr(s) is High(s), each FET of both of a charge pump is in an OFF state, and the capacitor of a low-pass filter (12) holds fixed potential, and holds a lock. However, when Pu is set to Low, the capacitor of a low-pass filter (12) is made to charge, and when Pd is set to Low, the capacitor of a low-pass filter is made to discharge. In this way, the always stabilized oscillation frequency can be obtained from a voltage controlled oscillator.

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EFFECT OF THE INVENTION

[Effect of the Invention] Since the processing inside a charge pump (6) is a digital signal, the digital control which used a microcomputer, RAM, the logical element, etc. is easy. This storage and control can perform power saving and temperature compensation. Moreover, a PLL synthesizer strong against a noise can be supplied.
[0030] Furthermore, in order to shorten lock-up time, two charge pumps are formed and the cure which changes this, or prepares two resistance and changes this is not needed.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Since the conventional charge pump consisted of FET of the above analogs, it was not easy to control by the control circuit or to memorize the value of a charge pump. For this reason, based on the value of a charge pump, control of PLL operation, such as power saving and temperature compensation, was difficult. Moreover, since control of a charge pump was difficult, the conventional PLL control had the problem of taking lock-up time for a long time, when a change of a division ratio was made greatly, in order to start feedback control from the state at that time, when a change of a division ratio is made.
[0004] Furthermore, since the charge pump of the conventional example had amended the control voltage of a low-pass filter by charge and electric discharge like ****, the time constant of a low-pass filter (12) needed to be changed to shortening lock-up time. For this reason, as shown in drawing 8 , a charge pump (15) and two (16) were prepared, this needed to be changed by the CONT signal, and two resistance needed to be prepared and this needed to be changed with a switch (17).

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] this invention was made in view of this point, and the 1st feature is that a charge pump consists of a counter which counts the phase contrast of the aforementioned rise signal Pu and the down signal Pd, a latch holding the output value of this counter, and a digital analog converter which changes the output of this latch into an analog signal.

[0006] The 2nd feature is having had the control circuit which controls change of the aforementioned control voltage based on a storage means memorizing the data concerning the output of the aforementioned counter, and this storage means.

[0007] The 3rd feature is having the control circuit which has by the output value of the aforementioned counter corresponding to the division ratio changed based on the aforementioned storage means, and controls the aforementioned latch, when a storage means to memorize the correlation of the output value of the aforementioned counter and the division ratio of a programmable divider, and change of a division ratio are.

[0008] It is the 4th feature's being equipped with a storage means, outputting the output of the latch which the aforementioned control circuit's made the aforementioned storage means memorize the output of a latch, and was memorized by the aforementioned storage means to a digital analog converter, and intercepting at least one between a voltage controlled oscillator and a digital analog converter.

[0009] It is holding the output-control voltage of the aforementioned low-pass filter in front of power-saving operation by equipping the 5th feature with the control circuit to which power-saving operation is made to perform by making a programmable divider into non-actuation, and a storage means, and the aforementioned control circuit's making the aforementioned storage means memorize the output of the aforementioned counter in front of power-saving operation, and controlling the aforementioned latch based on the aforementioned storage means at the time of power-saving operation.

[0010] The 6th feature is having the control circuit which has by the output value of the aforementioned counter in a predetermined division ratio based on a storage means memorizing the correlation of the temperature of the reference frequency VCO in which temperature compensation's is possible, and the output value of the aforementioned counter in a predetermined division ratio and reference frequency VCO, and the aforementioned storage means, and carries out temperature compensation of the reference frequency VCO.

[Translation done.]

* NOTICES *

OPERATION

[Function] Storage of control or an output is easy and can constitute a charge pump. Thereby, temperature compensation of power saving which makes a programmable divider non-actuation, shortening of lock-up time, and the reference frequency VCO is carried out.

[Translation done.]

* NOTICES *

EXAMPLE

[Example] The example of this invention is explained based on drawing. Drawing 1 is the block diagram of a PLL synthesizer. (1) is a voltage controlled oscillator (VCO) and it outputs desired frequency outside. (2) is a programmable divider (P/D) and it carries out dividing of the output of a voltage controlled oscillator (1) in adjustable. (3) is a temperature compensated crystal oscillator (TCXO), and it can tune oscillation frequency finely. (4) is a counting-down circuit and it carries out dividing of the output of a temperature compensated crystal oscillator (3). (5) is a phase comparator (phi/D) and it outputs the phase contrast of the output fr of a temperature compensated crystal oscillator (3) by which dividing was carried out to the output fp of a voltage controlled oscillator (1) by which dividing was carried out, and detection of a lock. Phase contrast is outputted by the rise signal Pu and the down signal Pd. (6) is a charge pump and it changes the rise signal Pu from a phase comparator (5), and the down signal Pd into voltage. A charge pump (6) is aligned with a phase comparator (5), and it is called the phase comparator (7) of a wide sense. On the other hand, (5) which does not contain a charge pump (6) is a phase comparator in a narrow sense. Here, a phase comparator in a narrow sense is only called phase comparator.

[0013] A charge pump (6) consists of a clock pulse (8), an updown counter (Up/Down counter) (9), and a latch (Latch) (10) and a digital analog converter (11) (DAC). An updown counter (9) counts each phase contrast from the rise signal Pu from a phase comparator (5), and the down signal Pd. A clock pulse (8) sends out the reference pulse signal for the count of an updown counter (9). A latch (10) holds the output of an updown counter (9). That is, the output of an updown counter (9) is temporarily memorizable. A digital analog converter (11) changes into the voltage according to counted value the output of the latch (10) which is a digital signal. (12) is a low-pass filter (LPF) and amends the control voltage to a voltage controlled oscillator (1) based on the output voltage of a digital analog converter (11).

[0014] (13) is a control circuit and controls each part. (14) is storage meanses, such as RAM and ROM, and memorizes data required for operation of a control circuit (13). For example, the correlation of the division ratio to the output of an updown counter (9) or temperature is memorized.

[0015] 12 is a timing chart which shows operation of a phase comparator (5) and an updown counter (9). If the output fp of a programmable divider (2) and the output fr of a counting-down circuit (4) are inputted into a phase comparator (5), only while the phase of fp is progressing rather than fr, the rise signal Pu of a phase comparator (5) serves as Low, and while the phase of fp is behind fr, the down signal Pd of a phase comparator (5) serves as Low. The pulse width of Low of Pu and Pd shows the phase contrast of fp and fr. This pulse width is changed into the signal (Pu' and Pd') expressed with the pulse width of High by the clock pulse (8) and the logical element (an inverter and AND gate). An updown counter (9) counts the pulse number of this Pu' and Pd', and outputs the value as a DESHITARU signal. The digital-output signal of an updown counter (9) is held by latch (10), and is changed into the voltage (analog) according to counted value (phase contrast) by the digital analog converter (11). The control voltage of a low-pass filter (12) is amended on this voltage.

[0016] Thus, if the phase of fp is progressing rather than fr, while the control voltage of a low-pass filter (12) was raised and the phase of fp is behind fr, the control voltage of a low-pass filter (12) is dropped. In this way, the always stabilized oscillation frequency can be obtained from a voltage controlled oscillator.

[0017] The above is the basic composition and basic operation of this invention, and has the following features.

[0018] ** Since the charge pump of the conventional example had amended the control voltage of a low-pass filter (12) by charge and electric discharge, it needed to change the time constant of a low-pass filter (12) to shortening lock-up time. For this reason, as shown in drawing 8 , two charge pumps were formed, this needed to be changed, and two resistance needed to be prepared and this needed to be changed. However, since the charge pump of this invention generates direct voltage, and in order for the speedup / speed down of applied voltage to a voltage controlled oscillator (1) to be dependent on the speed of a clock pulse (8), it is not necessary to take into consideration the time constant of a low-pass filter (12), and it has neither a charge pump nor resistance doubly like before, or operation which changes this is not needed.

[0019] * Since the processing inside a charge pump (6) is a digital signal, the digital control which used a microcomputer, RAM, the logical element, etc. is easy.

[0020] ** When a change of a division ratio is made, in order to start [illegible] conventional PLL control takes lock-up time for a long time, when a change of a division ratio is made greatly. The control circuit (13) of this invention reads the correlation of a division ratio and the output value of an updown counter (9) from a storage means (14), when a setting change of a division ratio is made in a key stroke etc. (Y of S1), as shown in drawing 3 (S2). The tabular format of the updown counter (9) output value corresponding to the division ratio of it that is sufficient as a correlation, and the function by statistics, such as the least square method, is sufficient as it. By this correlation, the change value of the updown counter (9) corresponding to the change value of a division ratio is calculated, and this value is outputted to an updown counter (9) (S3). Feedback operation of PLL is performed by making this value into initial value (S4).

[0021] Furthermore, it has with the lock-up signal from a phase comparator (5) by the output value of (Y of S5), and the updown counter at this time (9), and the data of the aforementioned correlation of a storage means (14) are updated (S6). (study)

[0022] Unless it carried out operation by the loop conventionally, the convergence value of attenuation was not found. However, since an updown counter (9) and a latch (10) are digital signals, this invention can output the voltage assumed easily from a charge pump (6). For this reason, lock-up time can be shortened and especially the effect when a change of a division ratio is made greatly is greatest.

[0023] ** Since an output is digital, a clock pulse (8) and a latch (10) are easy for a control circuit (13) to input into the next circuit the output value which made the storage means (14) memorize this output value, and made it memorize. And even if it intercepts between a voltage controlled oscillator (1) and a charge pump (6), the control voltage of a low-pass filter (12) can be held.

[0024] For example, as shown in drawing 4 , if the lock signal from a phase comparator (5) is received (S7), a control circuit (13) will make a storage means (14) memorize the output value of a latch (10) (S8), will read this output value from a storage means (14), and will output it to a digital analog converter (11) (S9). And between a latch (10) and digital analog converters (11) is intercepted (S10), and between a phase comparator (5) and charge pumps (6) is intercepted (S11). Next, supply (not shown) of the power supply to a programmable divider (2) is intercepted, and this is made into non-actuation (S12).

[0025] Thus, although a loop is intercepted and a programmable divider (2) serves as non-actuation, the control voltage of a low-pass filter (12) can be held by the output value of the latch (10) memorized. And by intercepting a loop, even if the noise by change of a phase comparator (5) is lost and a noise arises, a noise cannot carry out a loop and a PLL synthesizer strong against a noise can be supplied. Furthermore, power consumption can be lessened by making a programmable divider (2) into non-actuation.

[0026] an above-mentioned example -- especially -- power consumption -- although the large programmable divider (2) was made into non-actuation, even if it makes a counting-down circuit (4), a phase comparator (5), and an updown counter (9) into non-actuation, the output-control voltage of a low-pass filter can be held

[0027] Moreover, although DAC (11) was controlled by the above-mentioned example based on the output value of a latch (10), based on the output value of an updown counter (9), you may control a latch (10) (9).

[0028] ** Carry out small change of the frequency outputted from reference frequency VCO with temperature. For this reason, the control circuit (13) makes the storage means (14) memorize the correlation of the output value of an updown counter, and the temperature of reference frequency VCO in a predetermined division ratio beforehand. And temperature compensation of the reference frequency VCO is carried out to the division ratio set up from the output value of an updown counter using the correlation read from the storage means (14). Thereby, a temperature control with a high precision becomes possible.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the example of this invention.
[Drawing 2] It is the timing chart of an example.
[Drawing 3] The lock-up time of the control circuit of an example is drawing showing early operation.
[Drawing 4] It is drawing showing operation which serves as power saving in the noise of the control circuit of an example strongly.
[Drawing 5] It is the block diagram showing the composition of the PLL synthesizer which has the conventional charge pump.
[Drawing 6] It is drawing showing the composition of the conventional charge pump.
[Drawing 7] It is the conventional timing chart.
[Drawing 8] It is the block diagram which took the measures which bring the conventional lock-up time forward.
[Description of Notations]
1 Voltage Controlled Oscillator
2 Programmable Divider
3 Temperature Compensated Crystal Oscillator
4 Counting-down Circuit
5 Phase Comparator
6 Charge Pump
7 Phase Comparator
8 Clock Pulse
9 Updown Counter
10 Latch
11 Digital Signal Converter
12 Low-pass Filter
13 Control Circuit
14 Storage Means

[Translation done.]

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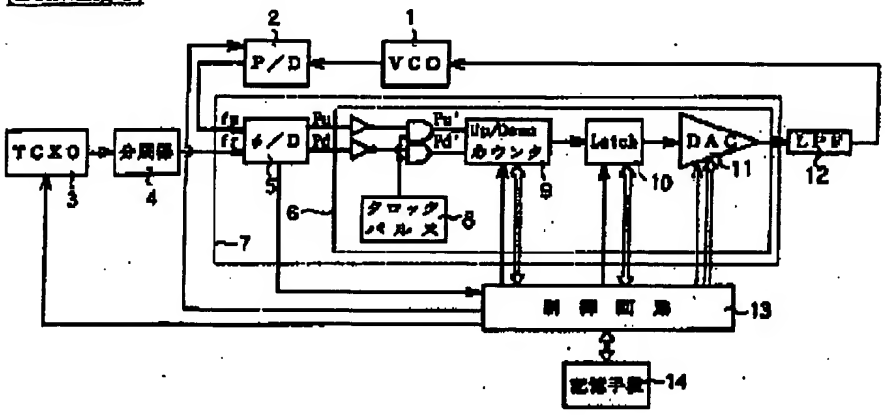
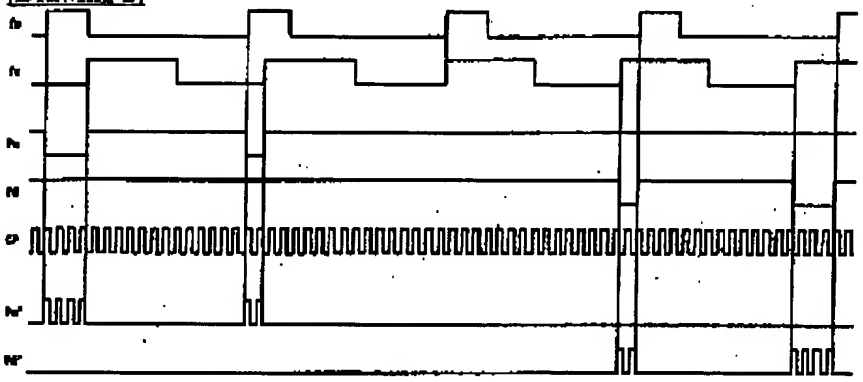
DRAWINGS

[Drawing 1]

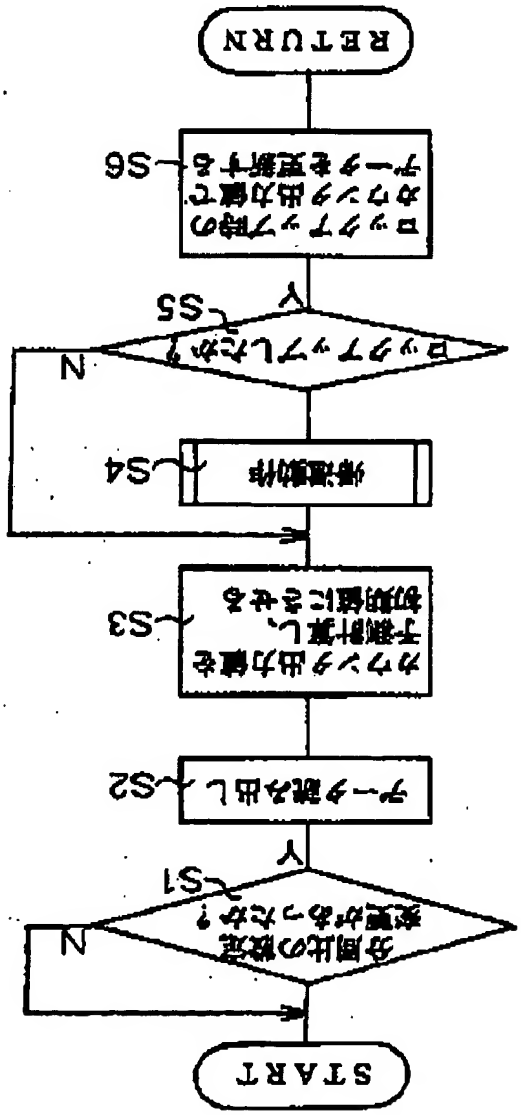


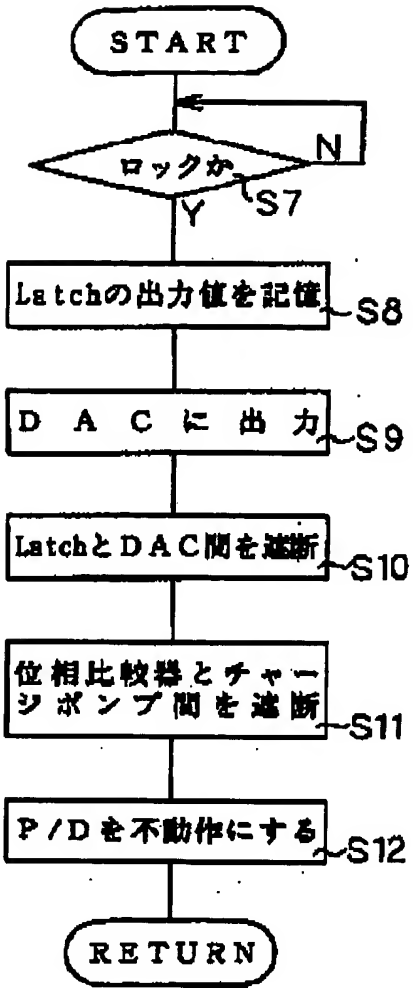
[Drawing 2]



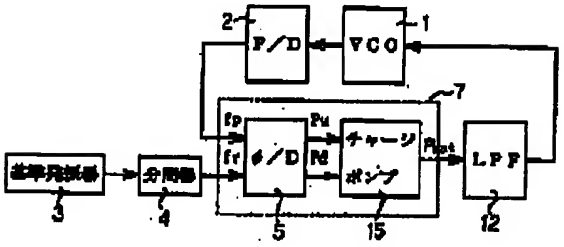
[Drawing 3]

Drawing 4

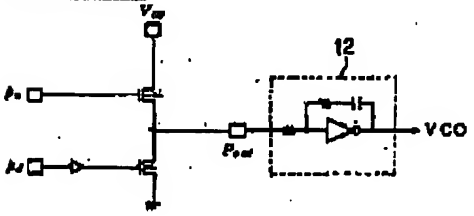




[Drawing 5]



[Drawing 6]



[Drawing 7]

[Translation done.]

[Drawing 8]